What is claimed is:

1. A nonvolatile semiconductor memory device comprising:

a substrate;

a semiconductor channel forming region in the vicinity of the surface of the substrate;

a first and a second impurity regions formed in the vicinity of the surface of the substrate sandwiching the channel forming region between them, acting as a source and a drain in operation;

a gate insulating film stacked on the channel forming region, and comprised of a plurality of films;

a gate electrode formed on the gate insulating film;

a charge storing means which is formed in the gate insulating film dispersed in the plane facing the channel forming region and in the direction of thickness and is injected with excited hot electrons in operation due to an electric field applied; and

wherein a bottom insulating film positioned at the bottom in said gate insulating film comprises a dielectric film that makes an energy barrier between the bottom insulating film and the substrate lower than that between silicon dioxide and silicon.

2. A nonvolatile semiconductor memory device as

set forth in claim 1, wherein said bottom insulating film comprises a dielectric film that makes an energy barrier between the bottom insulating film and the substrate lower than that between silicon and an oxynitride film formed after silicon dioxide is nitrided.

3. A nonvolatile semiconductor memory device as set forth in claim 2, wherein the percentage of nitrogen content in said oxynitride film is not greater than 10%.

4. A nonvolatile semiconductor memory device as set forth in claim 1, wherein in a write or erasure state, said charge storing means is primarily injected with anyone of channel hot electrons, ballistic hot electrons, secondarily generated hot electrons, substrate hot electrons, and hot electrons caused by band-to-band tunneling current.

5. A nonvolatile semiconductor memory device as set forth in claim 1, wherein said dielectric film included in said bottom insulating film exhibits a Fowler-Nordheim (FN) type tunneling electroconductivity.

6. A nonvolatile semiconductor memory device as set forth in claim 1, wherein said bottom insulating film includes said dielectric film comprised of anyone or a combination of a silicon nitride film, a silicon oxynitride film, a tantalum oxide film, a zirconium oxide film, an aluminum oxide film, a titanium oxide film, a

hafnium oxide, a barium strontium titanium oxide, and an yttrium oxide film.

7. A nonvolatile semiconductor memory device as set forth in claim 1, wherein, said gate insulating film comprises a nitride film or an oxynitride film exhibiting a Frenkel-Pool (FP) type electroconductivity on said bottom insulating film.

8. A nonvolatile semiconductor memory device as set forth in claim 1, wherein said gate insulating film comprises:

a first region into which the hot electrons are injected from said first impurity region;

a second region into which the hot electrons are injected from said second impurity region; and

a third region between the first and the second impurity regions into which the hot electrons are not injected.

9. A nonvolatile semiconductor memory device as set forth in claim 1, wherein said gate insulating film comprises:

a first region at the side of said first impurity region;

a second region at the side of said second impurity region; and

a third region between the first and the second

regions,

wherein said charge storage means is formed in the first and the second regions; and

wherein the distribution region of the charge storing means is spatially separated by the third region.

10. A nonvolatile semiconductor memory device as set forth in claim 9, wherein

said first and second regions are stacked film structures comprised of a number of films stacked together, and

said third region is a single layer of a dielectric.

11. A nonvolatile semiconductor memory device as set forth in claim 9, wherein a gate electrode formed on said third region is spatially separated from gate electrodes formed on said first region and second regions.

12. A nonvolatile semiconductor memory device as set forth in claim 1, comprising:

a plurality of memory transistors each of which including said channel forming region, said first and second impurity regions, said gate insulating film, and said gate electrodes, and arranged in both a word line direction and a bit line direction;

a plurality of word lines; and

a plurality of common lines which intersect with the plurality of word lines in an electrically insulated state,

wherein the plurality of gate electrodes are respectively connected to the plurality of word lines; and

wherein the plurality of the first and second impurity regions are coupled with the plurality of common lines.

13. A nonvolatile semiconductor memory device as set forth in claim 12, comprising:

word lines commonly connecting said gate electrodes in a word line direction;

first common lines commonly connecting said first impurity regions in a bit line direction; and

second common lines commonly connecting said second impurity regions.

14. A nonvolatile semiconductor memory device as set forth in claim 13, wherein:

said first common lines include

first sub-lines commonly connecting said first impurity regions in a bit line direction and

first main lines commonly connecting the first sub-lines in a bit line direction;

said second common lines include

second sub-lines commonly connecting said second impurity regions and

second main lines commonly connecting the second sub-lines; and

said plurality of memory transistors are connected in parallel between the first sub-lines and the second sub-lines.

15. A nonvolatile semiconductor memory device as set forth in claim 1, wherein said charge storing means does not have conductivity as a plane as a whole facing said channel forming region at least when there is not dissipation of charge in the outside.

16. A nonvolatile semiconductor memory device as set forth in claim 15, wherein said gate insulating film comprises:

a bottom insulating film on said channel forming region;

a nitride film or an oxynitride film on said bottom insulating film; and

a top insulating film on said nitride film or oxynitride film.

17. A nonvolatile semiconductor memory device as set forth in claim 15, wherein said gate insulating film comprises:

a bottom insulating film on said channel

forming region, and

a top insulating film on said bottom insulating film.

18. A nonvolatile semiconductor memory device as set forth in claim 17, wherein the Si-H bond density in the bottom insulating film is lower than that in the nitride film that shows a FP type electroconductivity and constitutes said top insulating film.

19. A nonvolatile semiconductor memory device as set forth in claim 18, wherein the Si-H bond density in the bottom insulating film is lower than $1x10^{20}$ atms/mm^3.

20. A nonvolatile semiconductor memory device as set forth in claim 19, wherein the Si-H bond density in the bottom insulating film is by more than one order of magnitudes lower than that in the nitride film showing a FP type electroconductivity and constituting said top insulating film.

21. A nonvolatile semiconductor memory device as set forth in claim 17, wherein said bottom insulating film comprises a buffer oxide film on said channel forming region and a dielectric film that is formed on said buffer oxide film and is comprised of a material having a dielectric constant greater than that of silicon dioxide.

22. A nonvolatile semiconductor memory device as

set forth in claim 17, wherein said bottom insulating film comprises:

a dielectric film formed on said channel forming region and comprised of a material having a dielectric constant greater than that of silicon dioxide and

a silicon dioxide film formed on the dielectric film.

23. A nonvolatile semiconductor memory device as set forth in claim 15, wherein said gate insulating film comprises:

a bottom insulating film on said channel forming region and

mutually insulated small particle conductors formed on the bottom film and functioning as said charge storing means.

24. A nonvolatile semiconductor memory device as set forth in claim 23, wherein said small particle conductors are of diameters not greater than 10 nanometers.

25. A nonvolatile semiconductor memory device comprising:

a substrate;

a semiconductor channel forming region in the vicinity of the surface of the substrate;

a first and a second impurity regions formed in the vicinity of the surface of the substrate sandwiching the channel forming region between them, acting as a source and a drain in operation;

a gate insulating film stacked on the channel forming region and comprised of a plurality of films;

a gate electrode formed on the gate insulating film; and

a charge storing means which is formed in said gate insulating film dispersed in the plane facing said channel forming region and in the direction of thickness and is primarily injected in operation with channel hot electrons, ballistic hot electrons, secondarily generated hot electrons, substrate hot electrons, and hot electrons caused by band-to-band tunneling current, and

wherein a bottom insulating film positioned at the bottom in the gate insulating film comprises a dielectric film of a material having a dielectric constant greater than that of silicon dioxide.

26. A nonvolatile semiconductor memory device as set forth in claim 25, wherein the Si-H bond density in said bottom insulating film is lower than that in a nitride film showing a FP type electroconductivity and constituting said gate insulating film.

27. A nonvolatile semiconductor memory device as

set forth in claim 26, wherein the Si-H bond density in said bottom insulating film is lower than $1x10^{20}$ atms/mm^3.

28. A nonvolatile semiconductor memory device as set forth in claim 27, wherein the Si-H bond density in said bottom insulating film is by more than one order of magnitudes lower than that in a nitride film showing a FP type electroconductivity and constituting said gate insulating film.

29. A nonvolatile semiconductor memory device comprising:

a substrate;

a semiconductor channel forming region in the vicinity of the surface of the substrate;

a first and a second impurity regions formed in the vicinity of the surface of the substrate sandwiching the channel forming region between them, acting as a source and a drain in operation;

a gate insulating film stacked on the channel forming region and comprised of a plurality of films;

a gate electrode formed on the gate insulating film; and

a charge storing means which is formed in said gate insulating film dispersed in the plane facing said channel forming region and in the direction of thickness and is primarily injected in operation with channel hot

electrons, ballistic hot electrons, secondarily generated hot electrons, substrate hot electrons, and hot electrons caused by band-to-band tunneling current,

wherein the gate insulating film comprises:

a first region at the side of the first impurity region;

a second region at the side of the second impurity region; and

a third region between the first and the second regions,

wherein said charge storage means is formed in the first and the second regions; and

wherein the distribution region of the charge storing means is spatially separated by the third region.

30. A nonvolatile semiconductor memory device as set forth in claim 29, wherein

said first and second regions are stacked film structures comprised of a number of films stacked together, and

said third region is a single layer of a dielectric.

31. A method for operating a nonvolatile semiconductor memory device comprising a substrate; a channel forming region of a semiconductor in the vicinity of the surface of the substrate; a first and a second

impurity regions formed in the vicinity of the surface of the substrate sandwiching the channel forming region between them and acting as a source and a drain in operation; a gate insulating film stacked on the channel forming region and comprised of a plurality of films; a gate electrode formed on the gate insulating film; and a charge storing means which is formed in the gate insulating film dispersed in the plane facing the channel forming region and in the direction of thickness and is primarily injected with hot electrons in operation, and a bottom insulating film positioned at the bottom in the gate insulating film comprising a dielectric film that makes the energy barrier between the bottom insulating film and the substrate lower than that between silicon dioxide and silicon,

said method comprising, in a write operation, a step of setting the voltage applied between the first and second impurity regions lower than that when the write speed is constant and the bottom insulating film is comprised of silicon dioxide.

32. A method for operating a nonvolatile semiconductor memory device as set forth in claim 31, comprising a step of setting said voltage applied between said first and second impurity regions not higher than 3.3 V.

33. A method for operating a nonvolatile semiconductor memory device as set forth in claim 31, comprising a step of setting said voltage lower than an energy barrier between silicon dioxide and said substrate at the side of conduction band.

34. A method for operating a nonvolatile semiconductor memory device as set forth in claim 31, comprising steps of:

reversing the application conditions of the bias voltage to said first and second impurity regions; and

performing a write operation again and injecting hot electrons into said charge storing means from either the side of said first or the side of the second impurity regions opposite to the side in said write operation.

35. A method for operating a nonvolatile semiconductor memory device as set forth in claim 31, wherein, in the distribution plane of said charge storing means facing said channel forming region, hot electrons injected from said first impurity region are localized and stored in the area at the side of the first impurity region.

36. A method for operating a nonvolatile semiconductor memory device as set forth in claim 34,

wherein, in the distribution plane of said charge storing means facing said channel forming region, hot electrons injected from said second impurity region are localized and stored in the area at the side of the second impurity region, when the application conditions of the bias voltage to said first and second impurity regions is reversed and a write operation is performed once again.

37. A method for operating a nonvolatile semiconductor memory device as set forth in claim 36, wherein, in said gate insulating film, the two storing regions of hot electrons injected from said first and second impurity regions are separated in two areas along the channel direction, sandwiching an intermediate region into which hot electrons are not injected.

38. A method for operating a nonvolatile semiconductor memory device as set forth in claim 31, comprising, in a read operation, steps of:

applying a specified read drain voltage between said first and second impurity regions while so as to make the source to be the impurity region at the side of the charge storing means to be read; and

applying a specified read gate voltage on said gate electrode.

39. A method for operating a nonvolatile semiconductor memory device as set forth in claim 34,

comprising, in a read operation, a step of reading more than two bits multi-bit data that are based on the hot electrons injected from said first and second impurity regions by changing the application direction of voltages to the first and the second impurity regions.

40. A method for operating a nonvolatile semiconductor memory device as set forth in claim 34, comprising, in an erasure operation, a step of extracting the charge injected from said first impurity region and stored in said charge storing means to the side of the first impurity region by utilizing the direct tunneling or the FN tunneling.

41. A method for operating a nonvolatile semiconductor memory device as set forth in claim 34, comprising, in an erasure operation, a step of extracting simultaneously or separately the charge, which are injected from said first and second impurity regions and stored in two separated areas near the two ends of said charge storing means in the channel direction, to the side of the substrate by utilizing the direct tunneling or the FN tunneling.

42. A method for operating a nonvolatile semiconductor memory device as set forth in claim 34, comprising, in an erasure operation, a step of injecting hot holes into said charge storing means from said first

and second impurity regions.

43. A method for operating a nonvolatile semiconductor memory device as set forth in claim 31, wherein said charge storing means does not have conductivity as a plane as a whole facing said channel forming region at least when there is not dissipation of charge in the outside.

44. A method for operating a nonvolatile semiconductor memory device as set forth in claim 43, wherein said gate insulating film comprises:

a bottom insulating film formed on said channel forming region;

a nitride film or an oxynitride film formed on the bottom insulating film; and

a top insulating film formed on the nitride film or oxynitride film.

45. A method for operating a nonvolatile semiconductor memory device as set forth in claim 43, wherein said gate insulating film comprises:

a bottom insulating film on said channel forming region and

a top insulating film on the bottom insulating film.

46. A method for operating a nonvolatile semiconductor memory device as set forth in claim 45,

wherein said bottom insulating film comprises:

a buffer oxide film on said channel forming region and

a dielectric film of a material which has a dielectric constant greater than that of silicon dioxide and is formed on the buffer oxide film.

47. A method for operating a nonvolatile semiconductor memory device as set forth in claim 46, wherein said bottom insulating film comprises:

a dielectric film of a material which has a dielectric constant greater than that of silicon dioxide and is formed on said channel forming region; and

a silicon dioxide film formed on the dielectric film.

48. A method for operating a nonvolatile semiconductor memory device as set forth in claim 43, wherein said gate insulating film comprises:

a bottom insulating film on said channel forming region; and

mutually insulated small particle conductors formed on the bottom film and functioning as said charge storing means.

49. A method for operating a nonvolatile semiconductor memory device as set forth in claim 48, wherein said small particle conductors are of diameters

not greater than 10 nanometers.